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(19)

(54) INTEGRATED CIRCUIT RECTIFIER

(71) We, HONEYWELL INC., a Corporation organised and existing under the laws of the State of Delaware, United States of America of Honeywell Plaza, Minneapolis, Minnesota 55408, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to integrated circuits and more particularly to providing a rectifier circuit in monolithic integrated circuits.

The desire to use, in monolithic integrated circuits, alternating voltages having negative peaks which would be the most negative voltages occurring in the circuit leads to a problem; this is the loss of isolation in those monolithic integrated circuits which use junction isolation techniques to electrically isolate the circuit device components therein. In one situation where this problem arises, an alternating voltage is to be rectified to provide an output voltage of constant polarity. Certain of the rectifier device components across which the negative voltage peaks occur will have (or tend to have) the junction isolating these components forward biased into conduction, in the absence of preventive measures, thus terminating the isolating properties of the junction. This, of course, is likely to cause disruption of the integrated circuit operation. A successful rectifier circuit for use in such an integrated circuit must somehow prevent the forward biasing to substantial conduction of isolation junctions when in operation.

A rectifier circuit which can accomplish the above has been disclosed in U.S. Patent 3,509,446 to Mullaly. However, to reach this accomplishment, the Mullaly patent shows using a pair of diodes plus a number of transistors and resistors. Also, the Mullaly circuit does not provide the constant polarity output voltage in a manner such that the substrate of the monolithic integrated circuit will be at the lowest voltage reached by this output voltage.

Accordingly the present invention provides an integrated circuit comprising a semiconductor layer having a rectifier component therein for rectifying an alternating voltage, a plurality of other components herein and an isolating region therein which isolates the rectifier component from the other components the threshold for conduction between this region and the cathode of the rectifying component being greater than the forward voltage drop across the rectifier component when conducting and a plurality of conductive paths on the surface of the semiconductor layer interconnecting the rectifier component and the other components, one of the conductive paths connecting the anode of the rectifying component directly to the isolating region.

The circuit may be a bridge rectifier having four similar rectifying components, sharing a common isolating region. In this case, two of the rectifying components will have their anodes connected together (forming the negative side of the output of the circuit), and it is these anodes which are connected to the isolating region. The forward voltage drop across whichever of these two rectifying devices is conducting is less than the threshold for conduction between the isolating region and the cathode of that rectifying device.

Two embodiments of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a top view of a monolithic integrated circuit;

Figure 2 is a corresponding circuit diagram;

Figure 3 is a section through the circuit of Figure 1; and

Figure 4 is a circuit diagram of a second circuit.

Figure 1 shows four metal-semiconductor diodes 10 to 13 individually formed in a monolithic integrated circuit. These diodes are Schottky or surface barrier diodes.

Shown with the diodes are the outlines of parts of the metallization for interconnections and input and output points. The metallization is not shown in full to avoid obscuring the remainder of the integrated circuit.

Metallization portion 14 connects the cathode of diode 10 to the anode of diode 11 and also to a terminal pad 14'. Metallization portion 15 connects the anode of diode 10 to the anode of diode 12 and to a terminal pad 15' which serves both as an output point and as a connector to the monolithic integrated circuit p-type conductivity substrate. Another metallization portion 16 connects the cathode of diode 12 to the anode of diode 13 and to a terminal pad 16' which forms an input point. Two joined metallization portions 18 form the direct voltage positive output point. The two portions 18 are connected together by a "crossunder" 17, and connect the cathodes of diodes 11 and 13 to one another. Truncated leadouts from metallization portion 18 and from metallization portion 15 feed the constant polarity output voltage to other electrical components (not shown) in the monolithic integrated circuit.

Figure 2 shows the effective electrical circuit provided by the structure shown in Figure 1. This circuit includes some added components not shown in Figure 1, namely diodes 28, 29, 30 and 31. These are parasitic diodes formed by the p-n junctions used to isolate the Schottky diodes described with respect to Figure 1.

The parasitic diodes of Figures 2 can be understood from Figure 3, which is a section view on line A-A of Figure 1 and includes one of the Schottky barrier diodes to show its construction. Only those parts of the metallization portions involved which actually make contact with circuit components in the monolithic integrated circuit are shown, i.e. interconnecting parts of the metallization are not shown in Figure 3.

Diode 10 is show, Figure 3, to be constructed in an n-type conductivity epitaxial layer, 25, formed over n^+-type conductivity buried layer region, 26, on a p-type conductivity substrate, 24. Diode 10 is junction isolated from the remainder of the integrated circuit by both a p^+-type conductivity region 19 to the right of the vertical dotted line, formed by diffusion, and by substrate 24.

These p or p^+-type conductivity isolation regions just mentioned, on the one hand, and the n^+ buried layer region 26 with that portion of epitaxial layer 25 adjacent thereto, on the other hand, effectively form the two sides of a parasitic p-n junction type diode for circuit description purposes. Thus a parasitic p-n junction diode is shown as diode 30 in Figure 2 and associated with Schottky diode 10. Each of the remaining Schottky diodes, diodes 11, 12, and 13 similarly have a parasitic p-n junction type diode associated therewith. In Figure 2, parasitic diode 31 is shown associated with Schottky diode 12, parasitic diode 28 is shown associated with Schottky diode 13 and parasitic diode 29 is associated with Schottky diode 11.

Returning to Figure 3, openings 22 and 23 (also shown in Figure 1) in a protective silicon dioxide layer, 27, permit interconnection metallization contact to that epitaxial layer portion which is involved in Schottky diode 10.

The metallization in opening 22 behaves as an ohmic contact as contacting region 20, provided through diffusion, has an n^+-type conductivity and this metallization serves as the contact 14 to the cathode of Schottky diode 10. The metallization shown in opening 23 forms the anode of Schottky diode 10 at its surface contact with epitaxial layer 25, while also serving as the electrical connection to this anode of Schottky diode 10.

A guard ring, 21, has a p-type conductivity and is formed by a diffusion prior to metallization. Guard ring 21 serves to increase the reverse breakdown voltage of Schottky diode 10 to 70 or 80 volts, thus allowing use of substantial voltages in the bridge rectifier circuit of Figure 2. If only relatively small voltages are to be used in the rectifier circuit, guard ring 21 need not be present.

The negative constant polarity voltage output point of the bridge rectifier circuit, formed by part of metallization portion 15, is shown in Figure 3 to the left of the vertical dotted line. This output point contacts substrate 24 through a p^+-type conductivity region which is formed as part of the isolating regions 19, also shown to the right of the vertical dotted line and mentioned above.

Turning to Figure 2, the alternating voltage is supplied between input points 14 and 16. A constant polarity output voltage is supplied to electrical loads, not shown, to be connected between output points 15 and 18. When input point 14 is positive with respect to input point 16, Schottky diodes 11 and 12 are forward biased into conduction while Schottky diodes 10 and 13 are back biased and do not conduct beyond a very small leakage current.

Although parasitic diode 31 becomes forward biased as point 16 is negative with respect to point 15, it does not become sufficiently forward biased to conduct any substantial current. This is because the forward drop across Schottky diode 12 required for this diode to conduct a substantial forward current is well below the forward conduction threshold voltage of diode 31 which has to be exceeded for diode 31 to conduct a substantial amount of forward current.

Reversing the polarity of input point 14 with respect to input point 16 places Schottky diodes 13 and 10 in forward conduction, again without parasitic diode 30 having a sufficient forward voltage drop across it to conduct a substantial amount of current. Regardless of the polarities of input points 14 and 16 relative to one another, output point 15, and so the substrate of the monolithic circuit, are always negative with respect to output point 18 and never more than a Schottky diode voltage drop above either of the input points 14 or 16 (at least at the peaks of alternating input voltages having a sufficient magnitude). Parasitic diodes 28 and 29 are thus always reverse biased.

It follows that the substrate is never more than one Schottky diode voltage drop above the lowest voltage appearing in the circuit. Thus, no isolating junctions become sufficiently forward voltage biased to conduct a substantial amount of forward current to thus permit undesired interactions between device components of the monolithic integrated circuit including those provided in this full-wave rectifier circuit.

A half-wave rectifier circuit having similar properties can also be constructed in a monolithic integrated circuit, as shown in Figure 4. The input points, 40 and 41, have an alternating polarity input voltage supplied to them. A half-wave rectified output voltage to supply loads in the monolithic integrated circuit appears between the output points, 42 and 43. Output point 43 is connected to the anode region of the diode 44, formed in an epitaxial layer, and via an isolating region to the substrate of a monolithic integrated circuit. The voltage at this output point is at the lowest potential supplied by the input voltage or one Schottky diode drop above this potential, depending on which half-cycle the input voltage is in, at least at the peaks of alternating voltages of sufficient magnitude. This is due to the rectifying properties of the Schottky diode 44. Schottky diode 44 is constructed in the same manner as diode 10 in Figure 3 and so has a parasitic diode associated with it, diode 45. Again, the parasitic diode 45 does not conduct during operation as its forward conduction voltage threshold is greater than the forward drop across Schottky diode 44 in conduction.

WHAT WE CLAIM IS:—

1. An integrated circuit comprising: a semiconductor layer having a rectifier component therein for rectifying an alternating voltage, a plurality of other components therein, and an isolating region therein which isolates the rectifying component from the other components, the threshold for conduction between this region and the cathode of the rectifying component being greater than the forward voltage drop across the rectifier component when conducting; and

a plurality of conductive paths on the surface of the semiconductor layer interconnecting the rectifier component and the other components, one of the conductive paths connecting the anode of the rectifying component directly to the isolating region.

2. An integrated circuit according to claim 1 wherein the semiconductor layer includes three further rectifier components connected with the first to form a bridge rectifier, the isolating region isolating all the rectifier components from each other and from the other components in the layer.

3. An integrated circuit according to either previous claim wherein the or each rectifier component is a Schottky diode.

4. An integrated circuit substantially as herein described with reference to Figs. 1 to 3 or Fig. 4 of the accompanying drawings.

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2 SHEETS

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SHEET 1

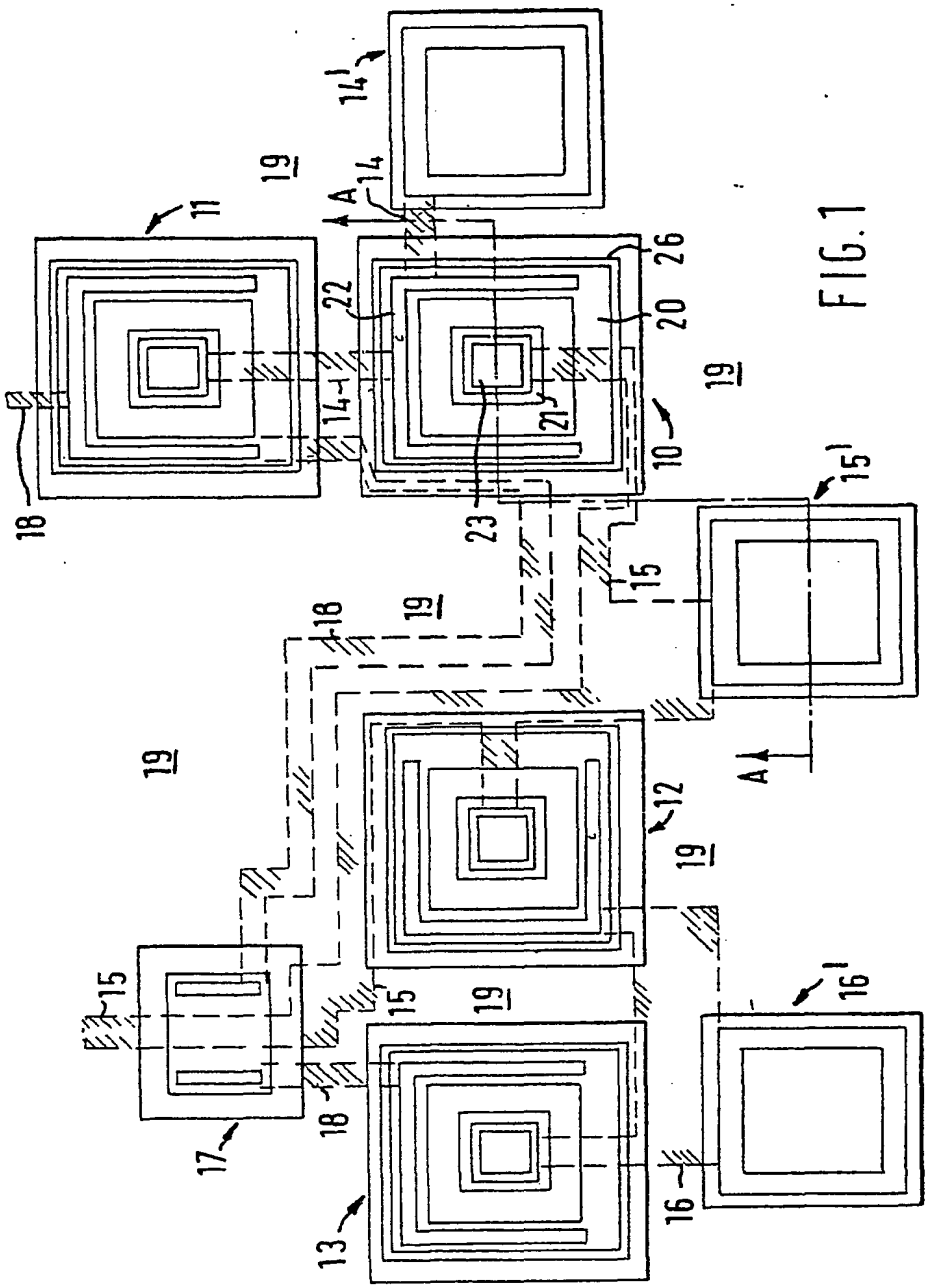

FIG. 1

1539784 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale.
SHEET 2

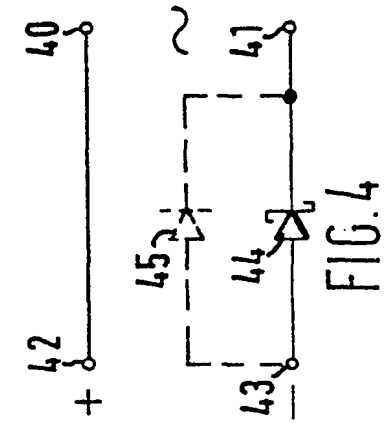

FIG.4

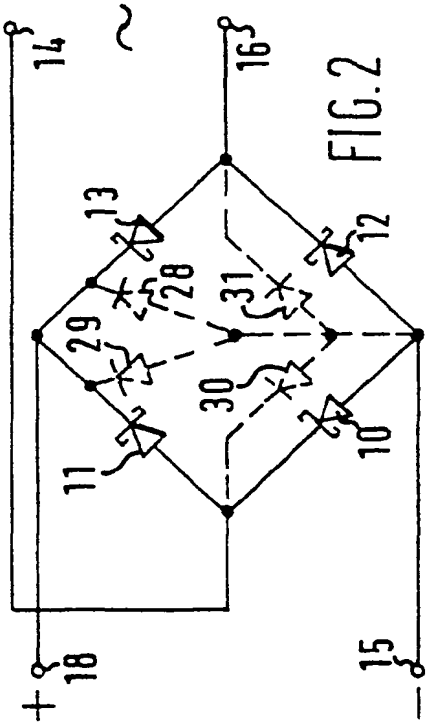

FIG.2

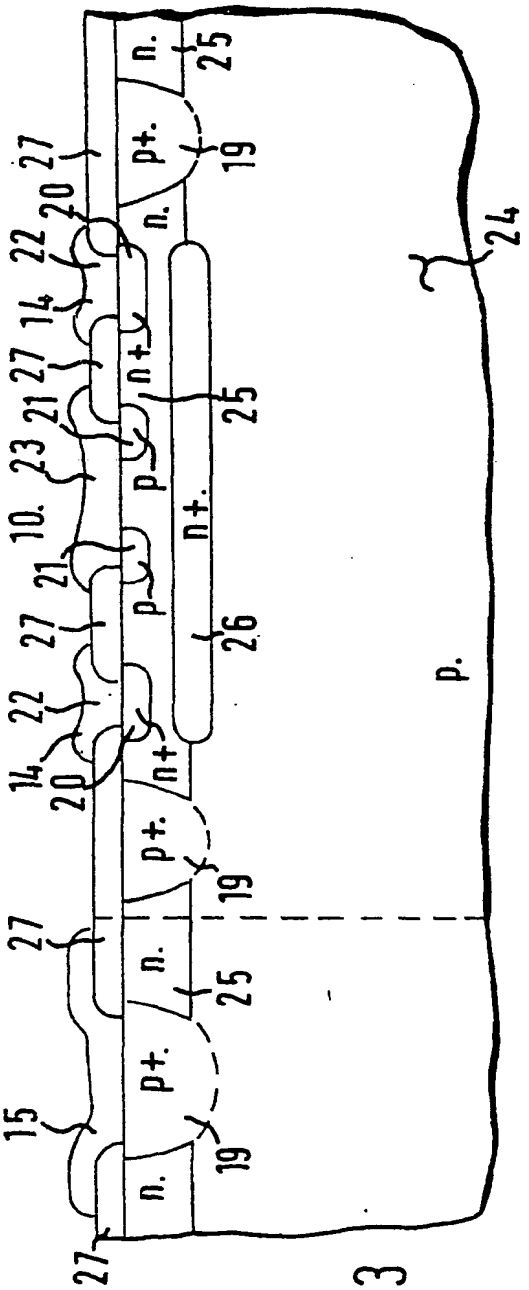

FIG.3

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